Innovation Drives the Evolution of Semiconductors

Semiconductor Production —A History of Innovation

In 1965, Dr. Gordon Moore, one of Intel's founders, made a prescient observation that eventually became Moore's Law. Six years later, Intel released the world's first commercial microprocessor, the Intel 4004. Over the following half century, through repeated technological innovation, semiconductor performance has continued to improve, with steadily higher circuit density realizing improved performance, such as increased capacity, speed and power efficiency.

Figure 1 illustrates the evolution of logic devices since 2000. In early planar poly-gates, strained silicon technology was introduced to improve channel mobility. Later, high-k[1]/metal gate technologies were introduced to reduce current leakage that arose due to miniaturization. To enhance pattern fidelity, circuit design transitioned from 2D layouts to combinations of simpler 1D layouts (Figure 2). As miniaturization continued beyond 45 nm, multiple patterning technologies were developed to compensate for the limits of lithography resolution, and FinFET structures were adopted to reduce short-channel effects. Going forward, with the advent of 5-nm technology and beyond, logic devices are expected to evolve into nanowire structures. In memory devices, the use of capacitors and transistors with 3D structures in DRAM have driven continued miniaturization, and the switch from planar NAND flash memory to 3D NAND has sidestepped the limits of miniaturization (Figure 3).

Through the combination of new designs and materials and the creation of new production methods, semiconductors have continued to evolve. Today, production technology is approaching the physical limits of miniaturization, at the atomic level. The world's first commercial microprocessor, manufactured with 10-micron technology, contained approximately 2,300 transistors per chip. In contrast, the latest mass-produced chips—products of 14-nm technology—boast well over a billion transistors per chip. The gate length on these chips is approximately 20 nm, and the width of the fins (the channels) is just 8 nm. Going forward, each successive technology node will entail miniaturization by a few nanometers, or the size of ten or so atoms. Manufacturing such devices will require atomic-level control.

1 High-k: High dielectric constant film

Technological Barriers to Miniaturization

Miniaturization in semiconductor production is now facing new hurdles. The first of these is photolithography resolution, a challenge that has emerged in recent years. Until now, miniaturization has advanced by using shorter wavelength light sources in exposure equipment to increase resolution. Today, however, the shortest wavelength available for use in mass production is 193 nm, more than 20 times the width

the aforementioned fins. The use of immersion lithography technology, in which exposure is conducted in a liquid medium with a high refractive index, helps to improve resolution, but even this is insufficient to achieve the desired results.

On top of this, aligning photomasks and wafers during patterning is also a challenge. In the latest logic and DRAM devices, transistors and other logic circuit elements are not only small, but arranged in complex configurations. If exposure alignment is off by a distance of just ten or so atoms, the densely arranged circuit elements will be interconnected inaccurately, leading to declines in processing precision.

Furthermore, at high-volume manufacturing sites, noise that always has a certain probability of occurring is becoming a more pronounced issue. The errors caused by such noise might not be problematic when lithography and etch processes are conducted just once. However, when lithography and etch processes are conducted multiple times on the same layer, these errors accumulate, leading to reduced yield. As miniaturization advances, these three challenges are expected to become even more serious. Solving them will be crucial to advancing to the 5-nm technology node and beyond.
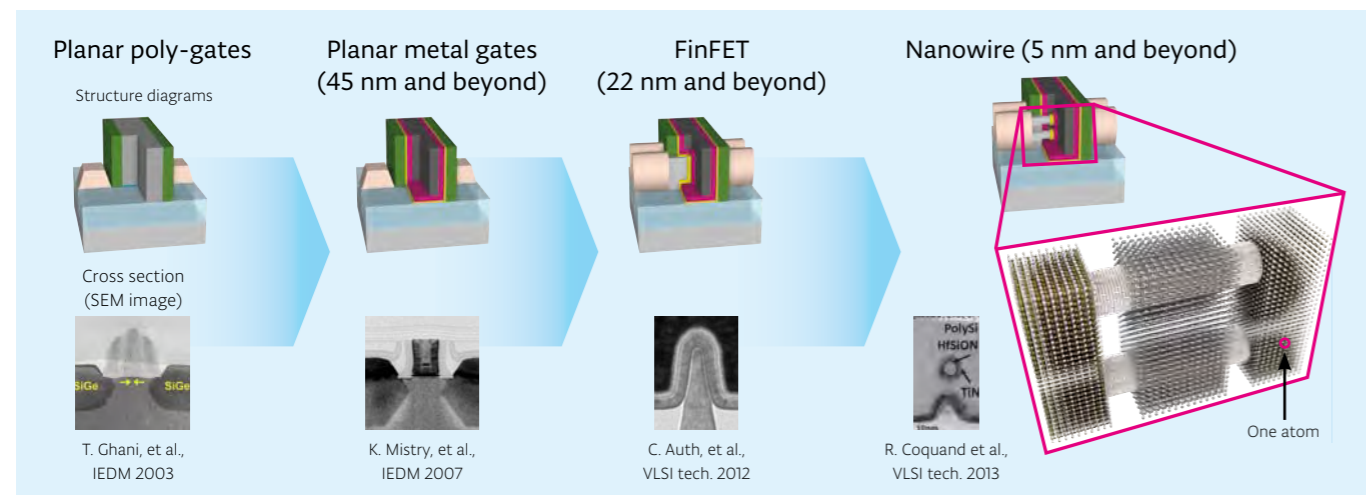
Breakthroughs in Production Technology

To solve these challenges, a number of breakthrough production technologies are beginning to emerge.

A well-known example, which is already widely used in mass production, is multiple patterning technology. This approach uses process technologies—such as deposition, lithography, etch and cleaning—to supplement the resolution of exposure equipment. Patterns with several times the density achievable by the lithography resolution can now be formed by employing the litho-etch method, in which lithography and etch processes are performed repeatedly, or self-aligned patterning, in which repeated deposition and etch processes are performed after lithography. These technologies are expected to see continued application in coming technology nodes. In addition, technology known as self-aligned block (SAB), which increases tolerance for placement variance in lithography, is currently being developed. By taking advantage of differences in etch selectivity by material, this technology is expected to enable the processing only of the desired materials without the need for improved performance from exposure equipment.
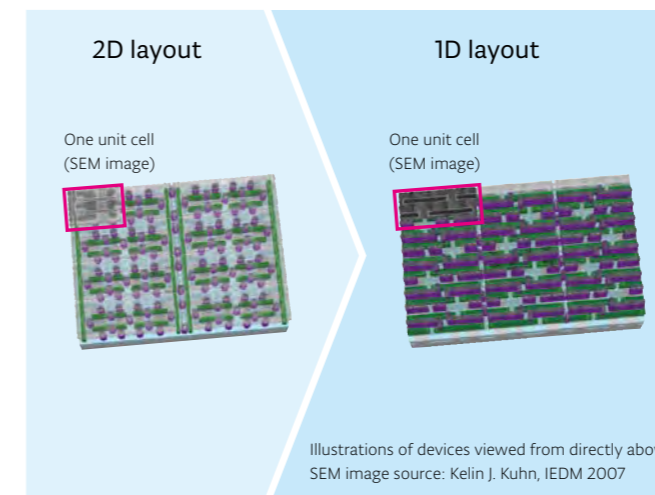
To realize these patterning technologies, the further refinement of production technologies for each unit process is indispensable. These include atomic layer etch (ALE) and atomic layer deposition (ALD), which control etching and deposition at the atomic level (Figure 4), as well as drying technologies to prevent pattern collapse caused by cleaning chemicals. In addition, the unit processes that give the best performance individually do not always achieve the highest yields when combined. This means that integration technology, aimed at optimizing unit processes to one

Figure 1. The Evolution of Logic Device Transistor Structures

Planar poly-gates
Structure diagrams
Cross section (SEM image)
T. Ghani, et al., IEDM 2003

Planar metal gates (45 nm and beyond)
K. Mistry, et al., IEDM 2007

FinFET (22 nm and beyond)
C. Auth, et al., VLSI tech. 2012

Nanowire (5 nm and beyond)
R. Coquand et al., VLSI tech. 2013
One atom

Devices evolved through changes in transistor materials and structure.
Manufacturing requires atomic-level production technology.

Figure 2. The Evolution of Logic Device Circuit Design

2D layout
One unit cell (SEM image)

1D layout
One unit cell (SEM image)

Illustrations of devices viewed from directly above
SEM image source: Kelin J. Kuhn, IEDM 2007

Miniaturization continued
by changing to simpler, 1D layouts.

Figure 3. The Evolution of NAND Flash Memory

Planar NAND flash (down to 15 nm)

3D NAND flash
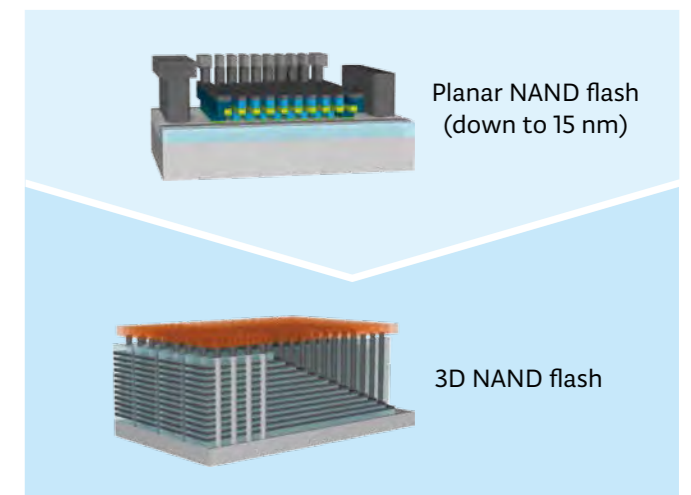
The method of increasing density changed
from planar miniaturization to vertical stacking.

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another, will only grow more important. Tokyo Electron provides equipment for a wide range of processes. Leveraging this strength, we are beginning to aggressively develop and offer integration technology solutions.
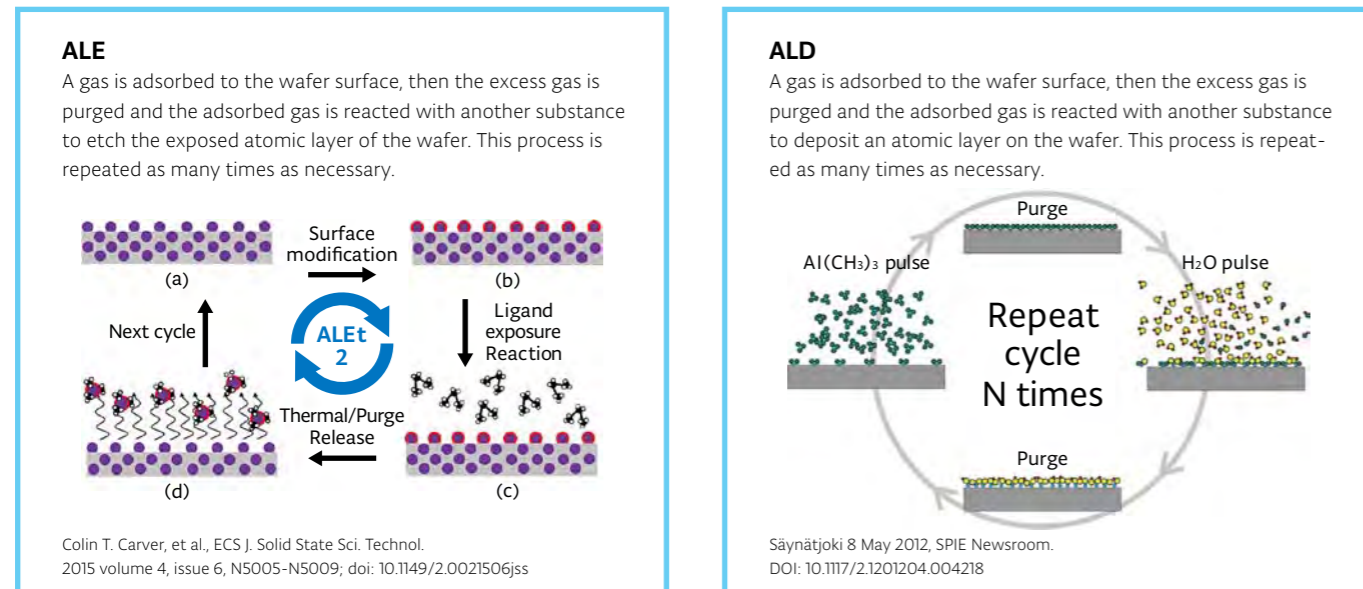
In addition to pattering technologies, EUV, a new type of light source for lithographic exposure, is approaching commercialization. In particular, the use of EUV in litho-etch processes (as explained above) is expected to reduce the number of masks needed per layer, reducing placement error and thereby increasing yields (Figure 5). Tokyo Electron is working with exposure equipment suppliers, consortia and other partners to develop coater/developers for EUV lithography. We report our progress every year at SPIE Advanced Lithography, the world's largest lithography conference, as we strive toward the adoption of EUV in mass production in the semiconductor industry. The combination of patterning technologies and EUV is now pushing miniaturization toward the 5-nm technology node and beyond.

excel in performing complex calculations on large volumes of information and are expected to be adopted in data center servers and similar electronics.

These new devices can only be commercialized through the application of existing semiconductor production technologies. Tokyo Electron is focusing not just on ways to continue miniaturization, but also on the technologies that will be required for continued evolution over the long term. In addition to our independent R&D initiatives, we are beginning to build an ecosystem for collaboration with consortia, academia and other equipment and material suppliers around the world. By creating new production technologies, Tokyo Electron will contribute to the continued evolution of semiconductors.

2 TS Böscke, et al., "Ferroelectricity in hafnium oxide thin films," Applied Physics Letters 99, 102903 (2011)

Figure 4: Atomic Layer Etch (ALE) and Atomic Layer Deposition (ALD)

ALE
A gas is adsorbed to the wafer surface, then the excess gas is purged and the adsorbed gas is reacted with another substance to etch the exposed atomic layer of the wafer. This process is repeated as many times as necessary.

(a) Surface modification (b)
Next cycle — ALEt2 — Ligand exposure Reaction
(d) Thermal/Purge Release (c)

Colin T. Carver, et al., ECS J. Solid State Sci. Technol. 2015 volume 4, issue 6, N5005-N5009; doi: 10.1149/2.0021506jss

ALD
A gas is adsorbed to the wafer surface, then the excess gas is purged and the adsorbed gas is reacted with another substance to deposit an atomic layer on the wafer. This process is repeated as many times as necessary.

Purge
$Al(CH_3)_3$ pulse H_2O pulse
Repeat cycle N times
Purge

Säynätjoki 8 May 2012, SPIE Newsroom. DOI: 10.1117/2.1201204.004218
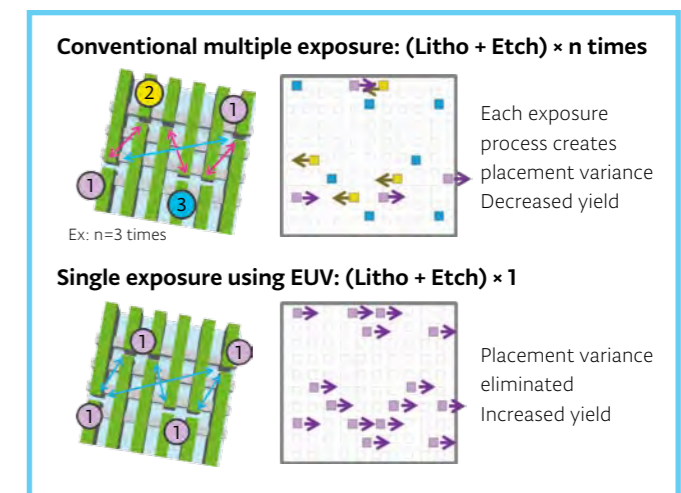
Beyond Miniaturization

Having reached the atomic level, semiconductor miniaturization is gradually approaching its physical limits. Nevertheless, semiconductor performance will continue to improve. Going forward, technological innovation will continue to advance in forms other than miniaturization.

In memory devices, ferroelectric memory (FeRAM) has been seen as a promising new type of memory since research on scalable ferroelectric materials was published in 2011.[2] In logic devices, research has begun into neuromorphic computers that employ new architectures known as non-von Neumann as well as quantum computers, which utilize quantum-mechanical phenomena. Neuromorphic computers require less energy to send electric signals than conventional devices. Because of this property, they are expected to reduce the power consumption of devices and be particularly suited to wearables and small IoT-related electronics. Quantum computers
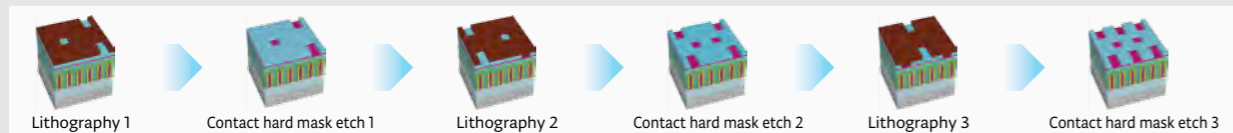
Column 01

Types of Multiple Patterning Technology

Multiple patterning technologies are broadly divided into litho-etch methods, in which lithography and etch processes are performed repeatedly on the same layer, and self-aligned patterning methods, in which repeated deposition and etch processes are performed after lithography. Litho-etch methods enable patterning density equivalent to that achievable based on the resolution of the lithography equipment multiplied by the number of litho-etch repetitions. This approach is well suited for reducing the pitch (the distance between features) of masks, such as those for forming contacts to connect transistors and wiring, vias to bridge the spaces between wiring, cuts to break lines formed by self-aligned multiple patterning, and blocks to fill spaces. Self-aligned multiple patterning, meanwhile, is useful for reducing the pitch of periodic line-space patterns. These techniques achieve patterning equivalent to twice the lithography resolution when performed once, and four times the lithography resolution when performed twice, which is why these approaches are referred to as double patterning (SADP) and quadruple patterning (SAQP), respectively.

**Litho-etch multiple patterning: Limited use of etch and deposition**

Lithography 1 — Contact hard mask etch 1 — Lithography 2 — Contact hard mask etch 2 — Lithography 3 — Contact hard mask etch 3

Self-aligned multiple patterning (SAMP): Performing etch/deposition numerous times

P — $\frac{1}{2}$P SADP — $\frac{1}{4}$P SAQP

Mandrel A etch — Sidewall deposition 1 — Sidewall etch back 1 — Hard mask etch — Mandrel B etch — Sidewall deposition 2 — Sidewall etch back 2

Figure 5. The Advantages of EUV Lithography in Litho-Etch Multiple Patterning Processes

Conventional multiple exposure: (Litho + Etch) × n times

Ex: n=3 times

Each exposure process creates placement variance Decreased yield

Single exposure using EUV: (Litho + Etch) × 1

Placement variance eliminated Increased yield

Column 02

Neuromorphic Computers

Neuromorphic computers are made by building chips that contain circuits that mimic human brain cells—neurons. When trained, these artificial neurons create synapses as they connect to one another, eventually forming a neural network. Compared with conventional semiconductor devices, such chips are expected to be more energy efficient. Moreover, if one neuron fails, its operation can instead be performed by another of the many neurons on the chip, making these chips highly reliable.

Synapse

Neuron
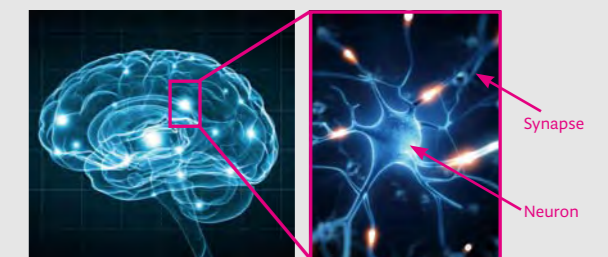
Conceptual illustration of a neural network